SCALABLE OPTIMAL TEST PATTERNS FOR CROSSTALK-INDUCED FAULTS ON DEEP SUBMICRON GLOBAL INTERCONNECTS

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Capacitance-coupling and mutual inductance between the neighboring wires of global interconnects give rise to crosstalk effects, which are one of the biggest signal integrity problems in DSM circuits today. Previous models for crosstalk-induced faults assume that all the wires of a bus act together to induce crosstalk effects on a single wire. Based on recent simulation results of Sirisaengtaksin and Gupta, we use a more general model of crosstalk-induced faults that allows tradeoffs between efficiency of tests and quality of tests. We construct provably optimal test patterns that covers all crosstalk-induced faults under this general model. Our test patterns admit simple generators for at-speed testing in BIST. The test methodology proposed here can result in huge savings in test cost. In particular, the required linear number of test patterns can be reduced to a constant number of test patterns by accepting only a few percent of error, thus allowing our test methodology to scale with bus width and technology.

Keywords: built-in self-test, crosstalk faults, DSM interconnects, fault model, test patterns

1. Introduction

The explosive growth of the Internet and the amount of data it has to handle have resulted in the need for dramatic performance increase throughout

the net. System designers are driven to increase device integration in the form of system-on-chips (SoCs), integrated CPUs, mixed signal and digital VLSI, as well as to decrease feature size so that systems remain deployable. Already, deep submicron (DSM) systems with feature size below 90nm are pervasive. This aggressive scaling of feature size leads to signal integrity problems, as the components are more susceptible to interference due to crosstalk, substrate noise, power bus noise, and distributed delay variations. Design techniques and validation[1–4] alone cannot deal with all of these errors because noise problems occur also in silicon, which only manifest themselves post-fabrication. Manufacturing testing therefore becomes a very important issue in DSM circuits. Unfortunately, the cost of testing is not scaling: while the cost of silicon manufacturing is decreasing with time, the cost of testing is actually increasing. New test paradigms have to succeed in order to change this situation. For this reason, testing has emerged as one of the most important areas of research in DSM technologies today.[5]

The focus of this paper is on testing crosstalk-induced failures on DSM global interconnects, particularly inter-core buses. Crosstalk-induced failures on these interconnects can give rise to logic errors and slowdowns/speedups.[6–9] Empirical data has shown that crosstalk effects are most significant in long interconnects.[10,11] Due to its timing nature, testing for crosstalk effect needs to be conducted at the operational speed of the circuit under test.[12] The built-in self-test (BIST) framework of testing is considered here as BIST is a more feasible solution for at-speed crosstalk testing.[13] In this framework, models for crosstalk faults are developed and test patterns that are likely to excite crosstalk faults in these models are generated by a processor and applied to the appropriate bus in the normal functional mode of the system. The bus under test is then observed for crosstalk faults under these test patterns. Many models have been considered for crosstalk in long DSM interconnects, but the one that has emerged as being not overly complex to analyze, yet remaining realistic, is the *maximal aggressor fault (MAF) model* of Cuviello *et al.*[10]

In the MAF model, a *victim* is a single wire of a set of interconnects. All of the other interconnects in the set are designated *aggressors*, which act collectively to generate errors on the victim via their coupling capacitances. The MAF model of Cuviello *et al.*[10] considered the four crosstalk-induced faults

(1) positive glitch (g_p),
(2) negative glitch (g_n),
(3) falling delay (d_f), and

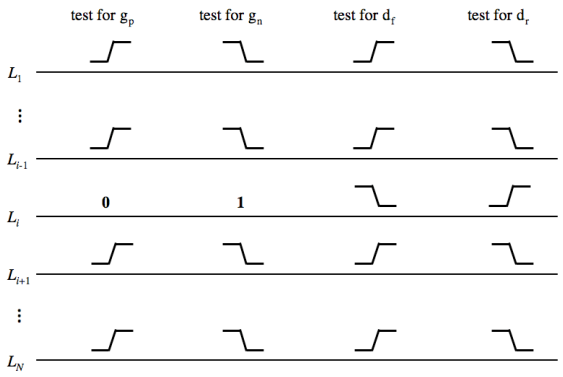

Fig. 1. Required transitions for the MAF model.

(4) rising delay (d_r).

The required transitions on the victim (line L_i) and aggressors to excite the four different possible faults are shown in Fig. 1. For example, to test for g_p on interconnect L_i, we need the two test vectors $\mathsf{u} = 0 \cdots 000 \cdots 0$ and $\mathsf{v} = 1 \cdots 101 \cdots 1$ (where the i-th component is at static 0) to produce the required transitions. We call $\mathsf{u} \rightarrow \mathsf{v}$ a *test pattern*. Under the MAF model, for a set of N interconnects, there are $4N$ faults to test, and we require $4N$ test patterns.

Our results in this paper generalize the MAF model to allow a tradeoff between efficiency of test and quality of test. We show how to generate the fewest test patterns to cover all crosstalk-induced faults under this generalized model. The number of test patterns required is less than the $4N$ required for the MAF model. If we accept a few percent of error, the required $4N$ test patterns can be reduced to a constant number. Our test methodology is therefore scalable.

2. Testing Under a Generalized MAF Model

Let $L_1, \ldots, L_N$ be a set of N linearly ordered interconnects, so that the neighbors of L_i are L_{i-1} and L_{i+1}, for $2 \leq i \leq N-1$, the neighbor of L_1 is L_2, and the neighbor is L_N is L_{N-1}. For $1 \leq s \leq N$, we define the *MAF model of strength s* (denoted s-MAF) as follows. A victim is a single interconnect as in the MAF model. However, we limit the number of aggressors to the s nearest interconnects on each side of the victim. The

faults under consideration are still g_p, g_n, d_r, and d_f. This is a justified model because the neighboring interconnects shield the victim from farther interconnects, and the capacitive coupling effect on the victim decreases with distance, as shown by Sirisaengtaksin and Gupta.[14] The MAF model of Cuviello *et al.*[10] is precisely the $(N-1)$-MAF model. Henceforth, we restrict our attention to $1 \leq s \leq N-2$. It is easy to see that any set of test patterns that covers all faults under the s-MAF model also covers all faults under the s'-MAF model, for all $s' < s$.

We now generate test patterns to cover the crosstalk-induced faults under the s-MAF model. We still have $4N$ faults to test for N interconnects. However, the number of test patterns required can be made smaller than the $4N$ required for the MAF model. In the MAF model, every test patterns covers only one fault, so $4N$ test patterns are necessary. Suppose $N = 8$. In the 2-MAF model, the test pattern $00000000 \rightarrow 11011011$ can test for g_p on victims L_3 and L_6 simultaneously. So fewer than $4 \cdot 8 = 32$ test patterns are required to cover all the 32 possible faults. Let us now formalize this observation.

For a vector u, u_i denotes the i-th coordinate of u. Let $\mathsf{u}, \mathsf{v} \in \{0,1\}^N$. A test pattern $\mathsf{u} \rightarrow \mathsf{v}$ can be encoded as a vector x over the set $\Sigma = \{0, 1, +, -\}$ as follows:

$$\mathsf{x}_i = \begin{cases} 0, & \text{if } \mathsf{u}_i = \mathsf{v}_i = 0, \\ 1, & \text{if } \mathsf{u}_i = \mathsf{v}_i = 1, \\ +, & \text{if } \mathsf{u}_i = 0 \text{ and } \mathsf{v}_i = 1, \text{ and} \\ -, & \text{if } \mathsf{u}_i = 1 \text{ and } \mathsf{v}_i = 0. \end{cases} \tag{1}$$

Any given vector over Σ can also be decoded uniquely to a test pattern $\mathsf{u} \rightarrow \mathsf{v}$. A vector over Σ is called an *encoded test pattern*. Given this equivalence between test patterns and encoded test patterns, we shall work with encoded test patterns, instead of test patterns, throughout this paper; their representation is more succinct and convenient.

Suppose that T is a set of encoded test patterns that covers all the faults under the s-MAF model. Let A be a $|T|$ by N array so that each row of A is an encoded test pattern of T. Then A has the following properties:

(1) if $N \geq 2s+1$, then in any $2s+1$ consecutive columns of A, each of the four vectors (the *in-between patterns*)

$$\begin{array}{ccccccc} + & \cdots & + & 0 & + & \cdots & + \\ - & \cdots & - & 1 & - & \cdots & - \\ + & \cdots & + & - & + & \cdots & + \\ - & \cdots & - & + & - & \cdots & - \\ \underbrace{\qquad\qquad}_{s} & & & & \underbrace{\qquad\qquad}_{s} & & \end{array}$$

appears in a row at least once;

(2) for $0 \leq t < s$, in the first $\min\{s+t+1, N\}$ columns of A, each of the four vectors (the *start patterns*)

$$\begin{array}{ccccccc} + & \cdots & + & 0 & + & \cdots & + \\ - & \cdots & - & 1 & - & \cdots & - \\ + & \cdots & + & - & + & \cdots & + \\ - & \cdots & - & + & - & \cdots & - \\ \underbrace{\qquad\qquad}_{t} & & & & \underbrace{\qquad\qquad}_{\min\{s,N-t-1\}} & & \end{array}$$

appears in a row at least once (ensuring that each wire with fewer than s neighbours to its left gets tested); and

(3) for $0 \leq t < s$, in the last $\min\{s+t+1, N\}$ columns of A, each of the four vectors (the *end patterns*)

$$\begin{array}{ccccccc} + & \cdots & + & 0 & + & \cdots & + \\ - & \cdots & - & 1 & - & \cdots & - \\ + & \cdots & + & - & + & \cdots & + \\ - & \cdots & - & + & - & \cdots & - \\ \underbrace{\qquad\qquad}_{\min\{s,N-t-1\}} & & & & \underbrace{\qquad\qquad}_{t} & & \end{array}$$

appears in a row at least once (ensuring that each wire with fewer than s neighbours to its right gets tested).

We call an array that satisfies these three properties a *crosstalk test array of length N and strength s*, and denote it by $\mathrm{CTA}(s, N)$. The number of rows of a $\mathrm{CTA}(s, N)$ is called its *size*. Our interest is in determining $\mathrm{CTA}(s, N)$ of small size, since the size corresponds to the number of encoded test patterns required.

The minimum size of a $\mathrm{CTA}(s, N)$ is denoted $\mathsf{C}(s, N)$. A $\mathrm{CTA}(s, N)$ is *optimal* if it has size $\mathsf{C}(s, N)$.

3. Optimal Crosstalk Test Arrays

We begin by establishing a lower bound on $\mathsf{C}(s, N)$.

Lemma 3.1.

$$\mathsf{C}(s,N) \geq \begin{cases} 4N & \text{if } N \leq s+1; \\ 4(s+1) & \text{if } N \geq s+2. \end{cases}$$

Proof. There are at exactly $4(s+1)$ distinct start patterns, and any CTA(s, N) must contain each of them as rows. So $\mathsf{C}(s, N) \geq 4(s+1)$.

When $N \leq s+1$, we have $4(s+1) \geq 4N$, giving $\mathsf{C}(s, N) \geq 4N$. □

We now describe a construction for crosstalk test arrays that meet the lower bound of Lemma 3.1.

Define the following vectors in $\{0, 1, +, -\}^{s+1}$:

$$\begin{array}{rcccccc} \mathsf{u}_{\mathrm{g_p}}(s) = & 0 & + & + & \cdots & + \\ \mathsf{u}_{\mathrm{g_n}}(s) = & 1 & - & - & \cdots & - \\ \mathsf{u}_{\mathrm{d_f}}(s) = & - & + & + & \cdots & + \\ \mathsf{u}_{\mathrm{d_r}}(s) = & + & - & - & \cdots & - \\ & & \underbrace{\qquad\qquad\qquad\qquad}_{s} & & & \end{array}$$

Let $\mathsf{M}_{\mathrm{g_p}}(s)$, $\mathsf{M}_{\mathrm{g_n}}(s)$, $\mathsf{M}_{\mathrm{d_f}}(s)$, and $\mathsf{M}_{\mathrm{d_r}}(s)$ be $(s+1)\times(s+1)$ circulant matrices whose first rows are given by $\mathsf{u}_{\mathrm{g_p}}(s)$, $\mathsf{u}_{\mathrm{g_n}}(s)$, $\mathsf{u}_{\mathrm{d_f}}(s)$, and $\mathsf{u}_{\mathrm{d_r}}(s)$, respectively.

For nonnegative integers s and t, now let

$$\mathsf{A}(s,t) = \underbrace{\begin{bmatrix} \mathsf{M}_{\mathrm{g_p}}(s) & \cdots & \mathsf{M}_{\mathrm{g_p}}(s) \\ \mathsf{M}_{\mathrm{g_n}}(s) & \cdots & \mathsf{M}_{\mathrm{g_n}}(s) \\ \mathsf{M}_{\mathrm{d_f}}(s) & \cdots & \mathsf{M}_{\mathrm{d_f}}(s) \\ \mathsf{M}_{\mathrm{d_r}}(s) & \cdots & \mathsf{M}_{\mathrm{d_r}}(s) \end{bmatrix}}_{t}.$$

Then $\mathsf{A}(s, t)$ is a $4(s+1) \times t(s+1)$ array over $\{0, 1, +, -\}$ (see Fig. 1 for an example of $\mathsf{A}(3, 8)$).

It is easy to verify that $\mathsf{A}(s, t)$ is a CTA$(s, t(s+1))$ of size $4(s+1)$ for any positive integer t.

Given $N \geq s+2$, let $t = \lceil N/(s+1) \rceil$. Then $\mathsf{A}(s, t)$ is a CTA$(s, t(s+1))$ of size $4(s+1)$ with at least N columns. Removing the last $t(s+1) - N$ columns from $\mathsf{A}(s, t)$ gives a CTA(s, N) of size $4(s+1)$. When $N \leq s+1$, $\mathsf{A}(N-1, 1)$ is a CTA(s, N) of size $4N$. Consequently, we have the following:

Theorem 3.1.

$$\mathsf{C}(s,N) = \begin{cases} 4N & \text{if } N \leq s+1; \\ 4(s+1) & \text{if } N \geq s+2. \end{cases}$$

Corollary 3.1. *Testing for crosstalk-induced faults on an N-bit bus under the s-MAF model can be accomplished with an optimal number of* $\min\{4(s+1), 4N\}$ *test patterns. These test patterns are explicitly given by the rows of an appropriately column-truncated* $\mathsf{A}(s, \lceil N/(s+1) \rceil)$.

4. Implementation

Our test methodology follows largely that of Chen *et al.*,[12] and focuses on testing for crosstalk-induced faults on inter-core data and address buses, as these are often long and wide and consequently most susceptible to crosstalk defects. Using this methodology, an embedded processor executes a self-test program, with which test patterns $\mathsf{u} \rightarrow \mathsf{v}$ (according to the optimal $\mathrm{CTA}(s,N)$ constructed in Section 3) are applied to the bus under test. In the presence of crosstalk-induced faults, v becomes distorted at the receiver end of the bus. The processor then stores this error effect to memory as a test response, which can later be unloaded for external analysis. The self-test program for our optimal test patterns under the s-MAF model has very low implementation and timing complexity due to the simple explicit circulant structure of the optimal $\mathrm{CTA}(s,N)$ we constructed.

Previous work have all focused on observing error effects on one victim per test pattern. Our test methodology under the s-MAF model allows us to observe multiple victims per test pattern. We describe how this can be done for inter-core data and address buses in the subsections below.

4.1. *Testing Data Buses*

Testing data buses is straightforward. To apply a test pattern $\mathsf{u} \rightarrow \mathsf{v}$ to a data bus from a core to the processor, the processor first exchanges u with the core. The processor then requests v from the core. Upon receiving v, the processor writes v to memory for later analysis. Since data buses are bidirectional, crosstalk effects vary as the bus is driven from different directions, so we also need to test the reverse direction. This can be done by having the processor send v to the core after exchanging u.

Identifying bus lines that are victims to crosstalk effects can be done as follows. Suppose that a test pattern $\mathsf{u} \rightarrow \mathsf{v}$ is applied and that v' is the final received vector written to memory. Let $x = \mathsf{v} \oplus \mathsf{v}'$, where $\oplus$ is the bitwise

XOR operator. Then the set of values of i for which $\mathsf{x}_i = 1$ indicates the lines that are victims.

4.2. *Testing Address Buses*

To apply a test pattern $\mathsf{u} \rightarrow \mathsf{v}$ to an address bus from the processor to a core, the processor first requests data from address u and v in two consecutive cycles. Since the processor addresses the cores via memory-mapped I/O, the processor will receive data from a different memory address or a different core if v is distorted to v' by crosstalk effects. To be able to identify this fault, the data stored in address v and the data stored in *all possible* v' must be different. Under the s-MAF model, our optimal test patterns can each observe $t = \lceil N/(s+1) \rceil$ victims. So there are altogether 2^t memory addresses, where we must store different values in order for us to identify which lines are victims to crosstalk-induced faults.

5. Significance

We have considered a generalized MAF model and constructed optimal test patterns under this model. We have also seen that our test patterns can be generated with a low-complexity program and results of tests are readily analyzed for victim wires. It remains to show that the s-MAF model, under which we achieved all these results are realistic. This has been done by Sirisaengtaksin and Gupta.[14] They observed that the contribution of lines to crosstalk effects at the victim line decreases as their distances from the victim increases. In particular, they obtained the simulation results in Table I for a 10000 micron long five-bit bus, where a *level j line* is one where there are j lines separating it from the victim line. Wires beyond level two contribute very little to crosstalk effects on the victim wire. In fact, based on these results, Sirisaengtaksin and Gupta suggested that if acceptable error criterion is set to a few percent, then the supporting lines at levels greater than two can be ignored for 0.18 micron CMOS technology.

If a similar error criterion is used, we need only test under the 3-MAF model. This can represent a huge savings in the cost of testing an N-bit bus, since $\mathsf{C}(3, N) = 16$ test patterns suffice to cover all crosstalk-induced faults under the 3-MAF model, regardless of how big N is. For example, under the MAF model, we require $4 \cdot 32 = 128$ test patterns to cover all crosstalk-induced faults in a 32-bit bus, whereas our test methodology requires only 16 test patterns, given by the rows of the array in Fig. 2. This is a 87.5% savings in the number of test patterns required. For a 64-bit bus, our test

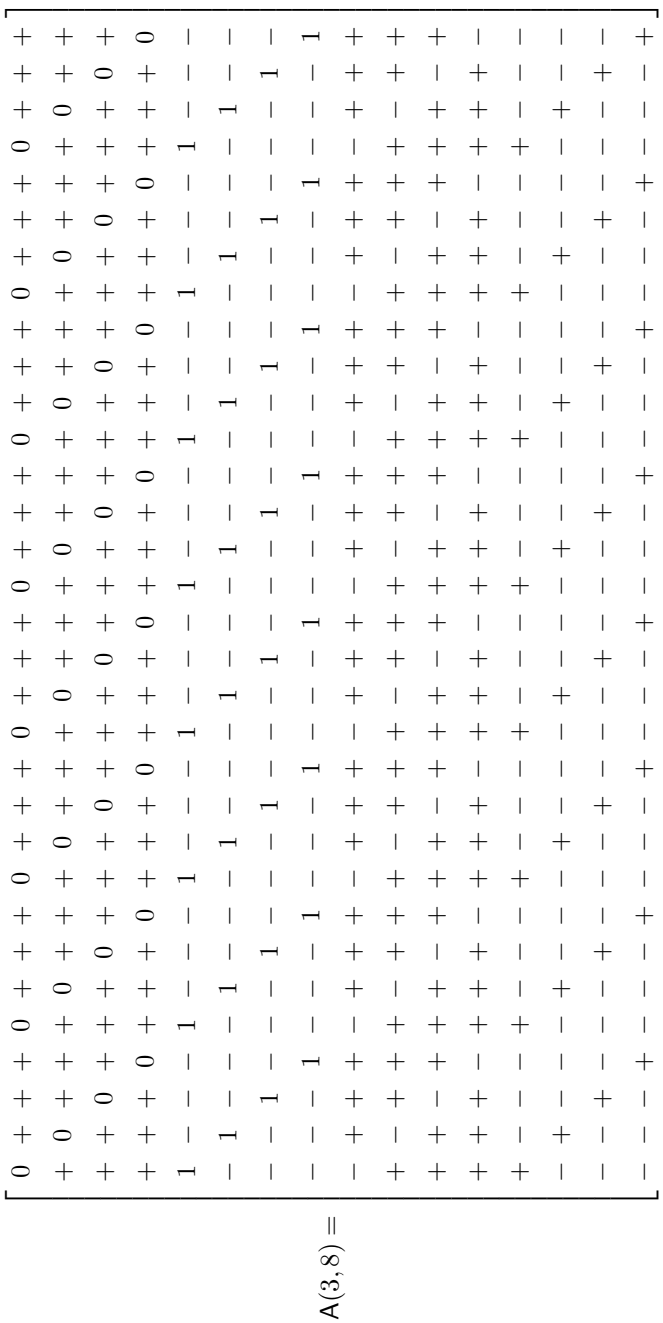

Fig. 2. The array A(3, 8), which is a CTA(3, 32).

methodology under the 3-MAF model results in over 93% savings.

Crosstalk effect	Level 1 line	Level 2 line	Level 3 line
Positive glitch	42.26%	10.87%	0.65%
Negative glitch	36.74%	15.28%	0.99%
Falling delay	25.08%	4.51%	1.55%
Rising delay	96.47%	35.69%	0.88%

The simulation results show that if we are willing to accept a few percent of error in testing, then crosstalk effects are a localized property. This allows our test methodology to scale regardless of the width of the bus under test. We do need, however, to adjust s according to feature size. As feature size reduces, the number of wires in close proximity to a victim increases, so s has to be increased. However, the simulation results of Table I shows that the contribution of these wires to crosstalk effects on the victim decreases rather rapidly.

6. Conclusion

In this paper, we considered a more general model for crosstalk-induced faults that allows for tradeoffs between test efficiency and test quality. Under this model, we constructed provably optimal test patterns for covering all crosstalk-induced faults. Our test patterns admit simple generators for BIST and can be used to obtain multitudes of savings in terms of test cost, by allowing only a few percent of error.

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