Light Emission From an Ambipolar Semiconducting Polymer Field-Effect Transistor

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ABSTRACT

Ambipolar light-emitting field-effect transistors are fabricated with two different metals for the top-contact source and drain electrodes; a low-work-function metal defining the channel for the source electrode and a high-work-function metal defining the channel for the drain electrode. A thin film of polypropylene-co-1-butene on SiN_x is used as the gate dielectric on an n^{++}-Si wafer, which functioned as the substrate and the gate electrode. Transport data show ambipolar behavior. Recombination of electrons and holes results in a narrow zone of light emission within the channel. The location of the emission zone is controlled by the gate bias.

Keywords: ambipolar, semiconducting polymer, field-effect transistor, light emission

1. INTRODUCTION

Several research groups have published results recently showing light emission within the channel of organic field-effect transistors (FETs), mainly for small molecules[1-6] but with some reports involving semiconducting polymers[7-10]. Generally, the bottom contact device geometry was used with gold as the metal for both the source and the drain electrodes.[1,2,4-5,7] Although light emission was observed near (or even slightly under) the negative drain electrode, these devices showed only hole transport. This is to be expected since electron injection from a high-work-function metal such as gold into the organic semiconductor would be limited by a large energy barrier.

Showing electron transport in polymer FETs had proven difficult until recently. Chua et al.[11] determined that hydroxyl groups serve as traps for electrons at the polymer-silicon dioxide (SiO_2) interface in FETs fabricated on Si with SiO_2 as the gate dielectric. By passivating the SiO_2, with pure, non-polar polymer dielectrics, electron transport was achieved in various conjugated polymers.

Efficient ambipolar injection in an FET requires the "two-color" electrode geometry, where the channel region of the transistor is defined by a low-work-function metal on one side and a high-work-function metal on the opposite side. Light emission in the channel region of an FET using the two-color electrode geometry was demonstrated[3,6,8-10]. Of those who employed the two-color electrodes, only Rost et al.[3] were able to show ambipolar behavior. Yet, the effect of the gate bias on the light emission was left unclear.

In this work, we report a semiconducting polymer light-emitting field-effect transistor (LEFET) fabricated by employing a new "angled" evaporation technique to deposit top-contact, two-color electrodes. Ambipolar transport was achieved by passivating the gate dielectric in a similar fashion to that reported on by Chua et al.[11] Under ambipolar conditions, recombination of electrons and holes resulted in the observation of a narrow zone of light emission within the channel. The emission zone moved across the channel as the gate bias was swept during collection of the transfer data.

2. EXPERIMENTAL PROCEDURE

2.1 Device fabrication and testing

To fabricate the devices, a heavily doped n-type silicon wafer was used as the gate electrode. The gate electrode was

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coated with 400 nm of silicon nitride (SiN_x) deposited by plasma enhanced chemical vapor deposition. The SiN_x surface was cleaned by sonication in acetone followed by an isopropanol rinse and further sonication in isopropanol. The device was then rinsed with ispropanol and dried under a stream of $N_{2(g)}$. The SiN_x was passivated with a thin film of polypropylene-co-1-butene, 14 wt. % 1-butene (PPcB), see Fig. 1b.

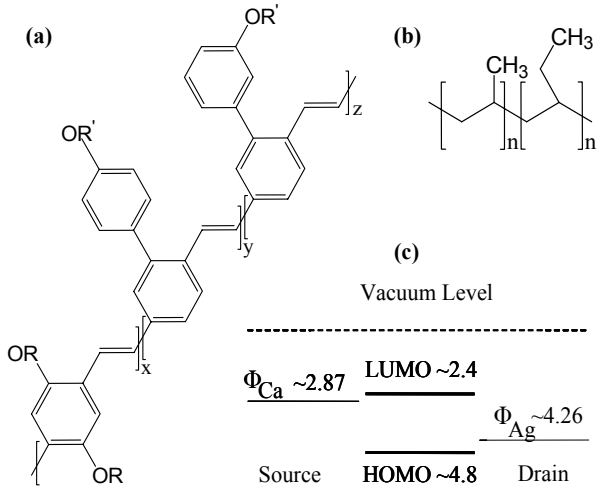

Figure 1: Molecular structure of (a) Super Yellow (SY) and (b) polypropylene-co-1-butene (PPcB). (c) Energy level diagram (units in eV) for the Ca source electrode/Super Yellow/Ag drain electrode device structure.

PPcB was obtained from Aldrich and used as received. 20 mg of PPcB were dissolved in 1 mL decaline at 190° C. The substrate was placed on a spin coater preset at 2500 rpm. The PPcB solution (at 190° C) was deposited onto the substrate. As soon as the PPcB solution covered the whole surface, the spin coater was turned on for 60 seconds. Uniform, 100 nm films of PPcB were obtained (thickness determined by Dektak profilimetry). After transferring the coated substrate into a nitrogen glove box, the PPcB film was then dried at 200° C for 3 minutes. "SuperYellow" (SY), a polyphenylenevinylene derivative obtained from Covion (see Fig. 1a), was spin cast onto the substrate at 3000 rpm. After the film deposition, the multilayer samples were annealed at 200° C for 30 minutes. The calculated capacitance of for the PPcB/SiN_x gate dielectric was 9 nF/cm^2.

The samples were mounted onto a silicon shadow mask in preparation for the angled evaporation technique, which is described below. Using the angled evaporation, Ca (Φ_{Ca} ~2.87 eV) and Ag (Φ_{Ag} ~4.26 eV) were deposited during the same pump down at ~1 x10^{-6} Torr to create the two-color electrode geometry. The resulting energy level diagram for SY is shown in Fig. 1c.

The devices were tested using a Signatone probing station that is housed in a nitrogen glove box. Oxygen count was ~ 1.5 ppm during device testing. A Keithley 4200 Semiconductor Characterization System was used to gather the electrical data while light emission was collected simultaneously with a Hamamatsu photomultiplier. For each run, the Ca electrode was always negative with respect to the Ag electrode. The channel region was imaged by focusing a Pulnix CCD camera on the channel through a 40x magnification microscope objective.

2.2 Silicon shadow mask fabrication

The top-contact, two-color electrode geometry was realized by developing a new, angled evaporation technique using silicon shadow masks. Two types of shadow masks have been demonstrated. In both cases, the masks were fabricated by starting with a silicon wafer with a 2 μm thick silicon oxide (SiO_2) layer. Holes were opened in the photoresist to expose the underlying SiO_2. A Panasonic Inductive Coupled Plasma Etching Sysemt was then used to etch SiO_2 down to the surface of the silcon wafer, yielding vertical sidewalls in the holes in the SiO_2 layer.

The 2 μm thick SiO_2 layer then served as an etch mask while etching holes through the 250 μm thick silicon wafer. The etching of the silicon wafer was done using the Bosch Etch Process in a Unaxis Silicon Deep Reactive Ion Etch Chamber. The Bosch Etch Process provides high fidelity to the SiO_2 etch mask, creating holes through the silicon wafer

with vertical side walls. The silicon is etched a rate of ~2 μm/minunte. SiO_2 is also etched by the process, but at a much slower rate. As it takes approximately 5 hours to etch through the silicon wafer, it has been found that the 2 μm thick SiO_2 layer is sufficiently thick to serve as an etch mask in this process and without being removed to expose the underlying silicon wafer.

Shadow Mask I is shown in Fig. 2. It was fabricated by etching two parallel rectangles (1000 x 100 μm) through a silicon wafer separated by a 20 μm "beam". The rectangles defined the electrode area, while the "beam" defined the channel region. As shown in Fig. 2, by evaporating at an angle, the shadow created by the "beam" enabled the fabrication of the top-contact, two-color electrode geometry. The devices reported on in this work used Shadow Mask I to deposit the two-color electrodes. These devices had a 16 μm channel length and a 1000 μm channel width. Channel lengths less than 5 μm have been achieved with this technique.

The schematic in Fig. 2 shows how the process by which Shadow Mask I is used to fabricate the top-contact, two-color electrode geometry by the angled evaporation technique: (a) The substrate is mounted on the silicon shadow mask and place at a set angle to the metal sources. The first metal, Ca, is evaporated. (b) The angle of the mask is changed with an electric motor, and the second metal, Ag, is evaporated. (c) The deposition of the two-color electrodes is complete; (d) The final structure of the two-color LEFET after the removal of the silicon shadow mask.

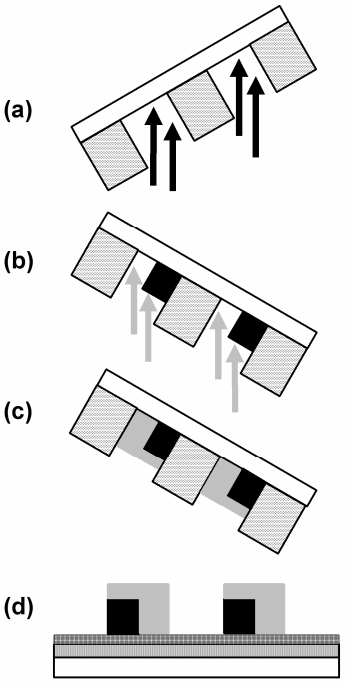

Figure 2: Shadow Mask I. Schematic of a top-contact two color electrode geometry fabricated using a silicon shadow mask where a central beam defines the channel length.

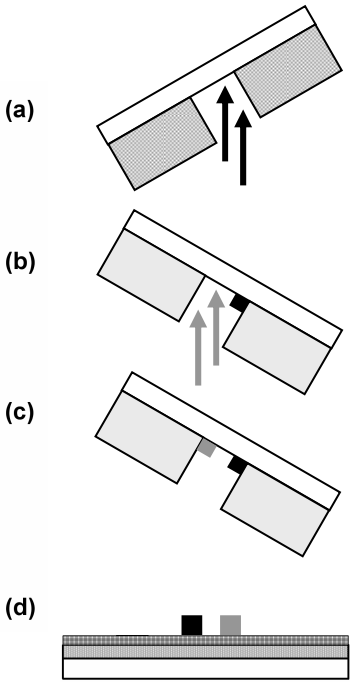

Figure 3:Shadow Mask II. Schematic of a top-contact two color electrode geometry fabricated using a silicon shadow mask where the channel length is defined by the angle of the evaporation.

Shadow Mask II is shown in Fig. 3. It was made by etching a narrow rectangle through the silicon wafer (40 μm by 10,000 μm). In this case, however, the shadow created by the silicon wafer is taken advantage of directly to define the channel region of the transistors. Fig. 3 depicts a similar fabrication process as described for Fig. 2. The angle of the silicon shadow mask with respect to the metal sources is chosen, such that the shadow created extends beyond the middle of the rectangular hole in the silicon wafer. The channel length for devices patterned using Shadow Mask II can be tuned through changing the angle of the silicon shadow mask. By precisely controlling this angle, it should be possible to obtain very short channels. To date, channels of about 5 μm have been fabricated using Shadow Mask II.

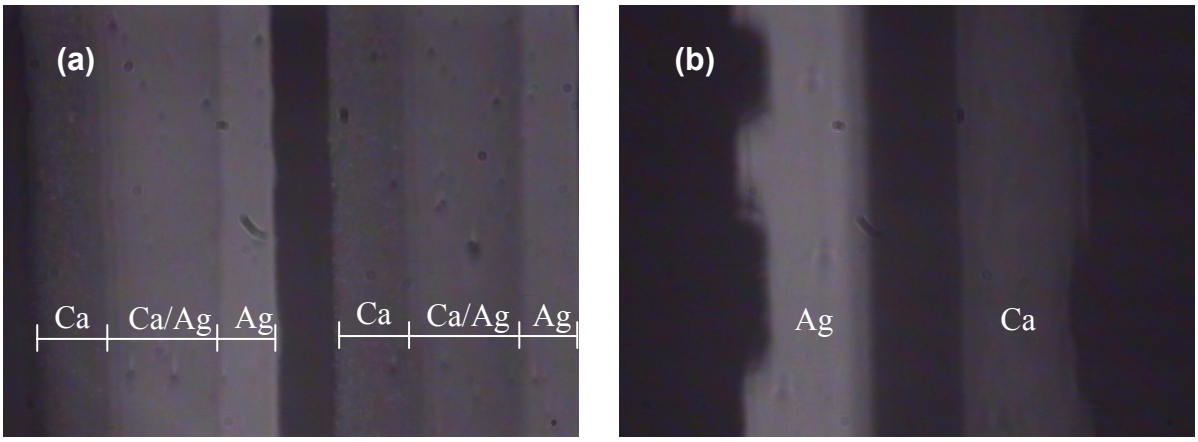

Figure 4: Micrographs taken at 40x magnification of two-color electrodes fabricated with (a) Shadow Mask I and (b) Shadow Mask II.

2.3 Defined gate using Shadow Mask II

A process has also been developed where Shadow Mask II can be used to deposit both the gate electrode and the two-color source and drain electrodes. Fig. 5 depicts this process: (a) shows the hole that is patterned and etched through the silicon wafer to make Shadow Mask II. (b) shows the patterned metal that results when a substrate is mounted on Shadow Mask II and the angle of evaporation is 90^{o} with respect to the metal source. This is the angle used to form the gate electrode. (c) depicts the formation of the top-contact, two color electrodes when the evaporation is done at an angle as described with Fig. 3 above. (d) shows the overlap of the gate electrode with the source and drain electrodes if they were stacked on top of each other.

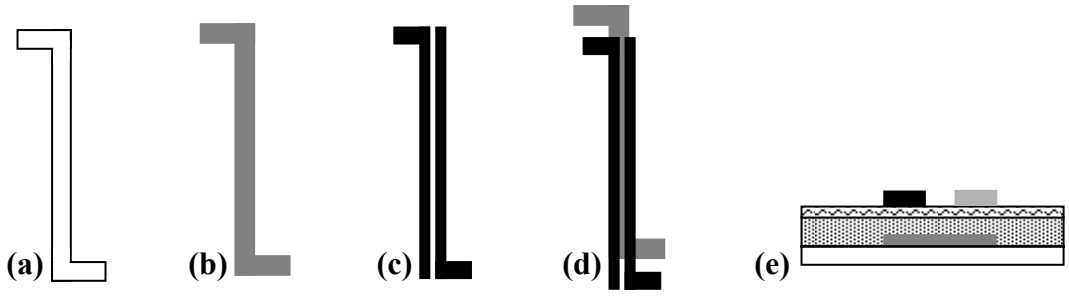

Figure 5: Use of Shadow Mask II to deposit both the gate electrode and top-contact, two-color source and drain electrodes.

Using this procedure, all the electrodes for the transistors can be patterned from the same silicon shadow mask. Different geometries can be employed using this design. The geometry we are focusing on is shown in (e). The gate electrode is first deposited. Then a gate dielectric, preferably a solution processible dielectric, is deposited and annealed on top of the gate electrode. The semiconducting polymer is then deposited by spin casting and annealed. The gate electrode on the substrate is aligned and fastened to Shadow Mask II using a microscope. The top-contact, two-color source and drain electrodes are then deposited by the angled evaporation technique.

Currently, the target channel length is 10 μm. Since the width of the rectangle through the silicon wafer that patterns the electrodes is 40 μm, the width of each electrode (the long bars on either side of the channel as shown in Fig. 5c) is 15 μm, which is also equal to the overlap with the gate electrode. By using Shadow Mask II and the process described herein, field-effect transistors structures with patterned gates that have small overlap with the source and drain electrodes have been realized. The reduction of this overlap will reduce leakage current through the gate dielectric, and should allow for the employment of thinner gate dielectrics films, resulting in an increase in the capacitance of the device and therefore, a reduction in the drive voltage. Now that this FET structure has been realized, current work is focusing on finding a solution processible gate dielectric that will support hole and electron transport and have low enough leakage current such that the devices function properly.

3. RESULTS

Transfer data (I_d vs. V_g scan) together with the gate dependence of the light emission representative of the fabricated LEFETs are shown in Fig. 6. The transfer scan was run with a constant drain voltage (V_d) of 200 V. The low-work-function source electrode (Ca) was grounded and the gate voltage (V_g) was swept from 0 to 200 V. When $V_g = 0$, there is no voltage drop between the source and gate. There is, however, a 200 V drop between the drain and gate which polarizes the gate dielectric and induces a hole channel in the vicinity of the high-work-function drain electrode (Ag). The current in this region (at lower V_g values) of the transfer scan is hole dominated.

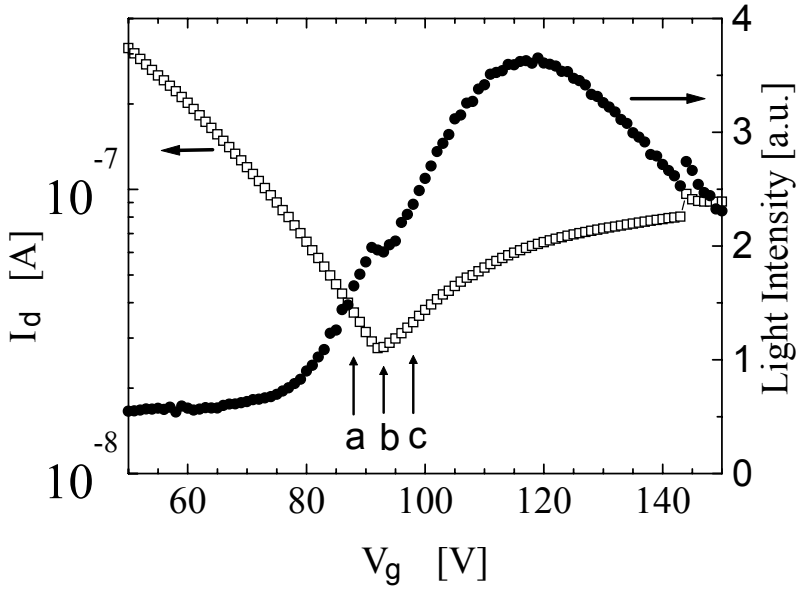

Figure 6: Transfer scan (I_d vs. V_g) for the SY LEFET along with the corresponding emitted light intensity vs. V_g. The emission zone is located in the channel: (a) near the Ca source electrode, (b) near the center of the channel, and (c) near the Ag drain electrode (see Fig. 7).

As V_g increases, the voltage drop between the drain and gate decreases, causing the magnitude of the hole current to decrease. Simultaneously, the voltage drop between the source and the gate increases, but is oppositely charged, causing the gradual buildup of an electron channel near the low-work-function source electrode (Ca). At about V_g= 90 V, I_d reaches a minimum and then begins to increase again. This is the crossover point from hole dominated current to electron dominated current. Crossover is expected to occur at V_g= ½ V_d, in good agreement with the data in Fig. 3.

The field effect mobility (μ) can be calculated from using the Equation 1.

$$I_d = \mu C_i \frac{W}{2L}\left(V_g - V_{th}\right)^2, \quad (1)$$

Equation 1 models the an FET while operating in the saturation regime. The devices tested in this work are considered to be operating in the saturation regime because $V_d > V_g$. In Equaition 1, C_i is the capacitance of the gate dielectric, V_{th} is the threshold voltage, W is the channel width, and L is the channel length. The resulting hole and electron mobilities are $\mu_h = 3 \times 10^{-4}$ cm^2/V/sec and $\mu_e = 6 \times 10^{-5}$ cm^2/V/sec. The electron mobility is lower than the hole mobility, which is likely due to residual electron traps that are still present after the PPcB passivation. The threshold voltage for electrons ($V_{th,e}$) is 57 V, and the threshold voltage for holes ($V_{th,h}$) is 110 V.

The light intensity data corresponding to the transfer scan is also shown in Fig. 6 also. The light intensity data begins increasing around 80V while hole current still dominates, reaching a maximum around 120 V, well into the electron dominated current regime. By employing the two-color electrode geometry, light emission should be observed when both electron and hole currents are simultaneously present during device operation, consistent with the light intensity vs. V_g data in Fig. 6. At the crossover point the hole and electron currents are nearly equal to each other, and the quantum efficiency for light emission is maximum. Note, however, that the light intensity peaks at V_g~120 V, i.e. when the

electron current is greater than the hole current. A higher electron current might be necessary to achieve maximum brightness because the higher density of electron traps would reduce the number of electrons available for recombination.

Images taken of the channel region during operation show the location and width of the emission zone are shown in Fig. 7. The emission was found to be in a very narrow region (< 2 μm) within the channel. The emission zone is not stationary within the channel, but in fact moves from the source to the drain as the gate voltage is swept from 88 V (a) to 93 V (b) to 98 V (c) in Fig. 6. Shown in Fig. 7 are photographs which image the position of the emission zone corresponding to points a, b, and c in Fig. 6. In Fig. 7a, the emission zone is close to the calcium source electrode.

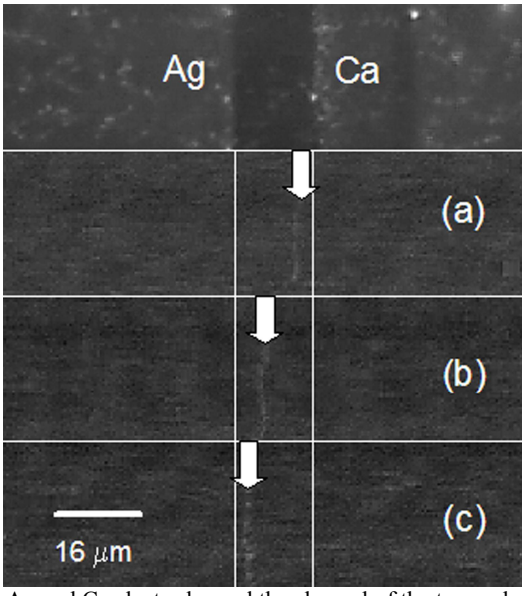

Figure 7: The top photograph shows the Ag and Ca electrodes and the channel of the two-color LEFET. Photographs (a), (b), and (c) are taken in the dark while the device is operating. The emission zone moves from near the Ca electrode, (a) V_g = 88 V, to mid-channel, (b) V_g = 93 V, and then approaches the Ag electrode, (c) V_g = 98 V.

As Vg increases, the emission moves across the channel (Fig. 7b), finally approaching the silver drain electrode (Fig. 7c). This gate induced shift in the emission zone from the source to the drain takes place over a small voltage range near the current crossover point. The emission line is near the center of the channel at the point where current crossover occurs.

3. DISCUSSION

Schmechel et al.[13] recently proposed a model for the operation mechanism of an ambipolar organic LEFET. They model the ambipolar field-effect transistor using an equivalent resistor-capacitor network. Their model is consistent with the discussion above. Their discussion begins by stating that the channel resistance is dependent upon the number of charge carriers in the channel. They then showed that the number of charge carriers in the device is related to the charge induced across the dielectric. Charge = Capacitance*V_g. Depending on the location within the channel, a different effective charge is induced, which is analogous to the discussion earlier in this work which stated that the number and type of charge carriers varies through the channel based on the biases applied at the gate, drain, and source electrodes. Schmechel et al.[13] introduce an equation which models the location of the recombination (emission) zone in an ambipolar LEFET. Shown below is an alteration of Equation 14 from the Schmechel et al.[13] work where additional terms have been introduced to account for the threshold voltages for both electrons and holes.

$$x_o = \frac{L\left(V_g - V_{th}^e\right)^2}{\left(V_g - V_{th}^e\right)^2 + \frac{\mu_h}{\mu_e}\left(V_d - \left(V_g + V_{th}^h\right)\right)^2}, \quad (2)$$

x_o is the location of the recombination zone and L is the channel length. The inclusion of the threshold voltages into Equation 2 for both electrons and holes provided a good fit between our data and the model as seen in Fig. 8. Using the model, $V_{th,e}$ and $V_{th,h}$ were found to be 75 V and 99 V respectively.

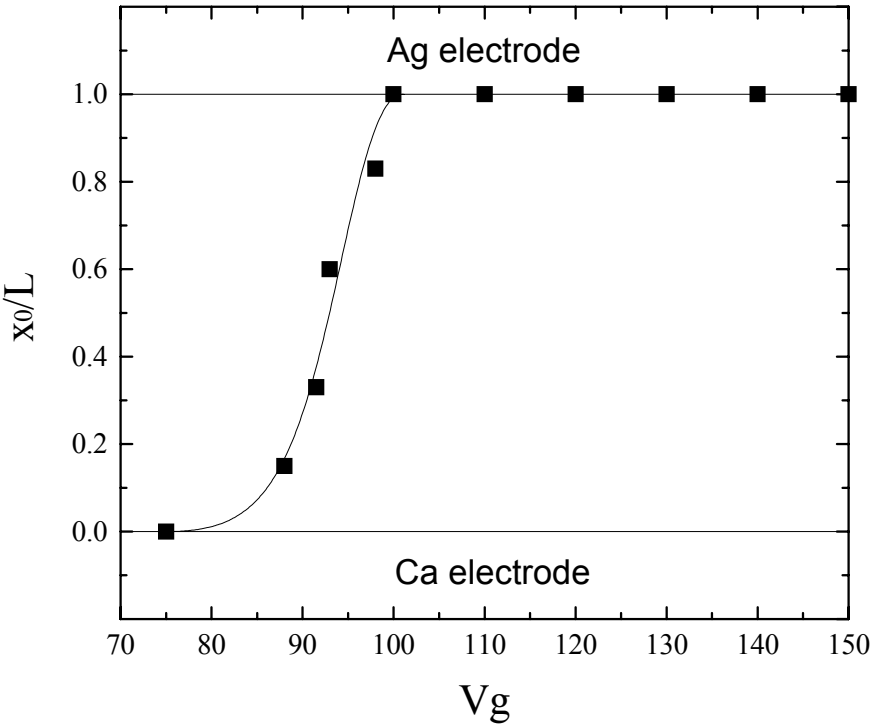

Figure 8: The location of the emission zone relative to the channel length (x_o/L) is plotted as a function of gate voltage. The symbols are the data points taken from the data set shown in Fig. 7. The solid line is the best fit to the data obtained by using Equation 2.

Table 1 shows the relationship found upon comparing the threshold voltages obtained from Equations 1 and 2. V_{th} values obtained from Equation 1 indicate the point in the transfer scan where charge transport begins. For $V_g < 57$ V, there is virtually no electron current, while for $V_g > 110$ V, there is virtually no hole current in the channel.

	Equation 1	Equation 2
$V_{th,e}$	57 V	75 V
$V_{th,h}$	110 V	99V

Table 1. Comparison of threshold voltages for both electrons and holes, as obtained from Equations 1 and 2.

The V_{th} values from Equation 2 are related to the movement of the location of the emission zone. When $V_g = V_{th,e,2} = 75$ V, the emission zone is very near the calcium source electrode. As V_g increases, the emission zone moves across the channel until very near the Ag electrode at $V_g = V_{th,h,2} = 99$ V. The emission zone could be said to traverse the entire length of the channel region rather quickly as it does so over a relatively small voltage range of 26 V, from $V_g = 75$ to 99 V. This is indeed a small range when considering the gate voltage is swept from 0 to 200 V.

In an ideal device with low charge trap density, the recombination zone (or emission zone), would be expected to travel more slowly across the channel region, i.e. for the whole voltage range of the gate voltage scan. The shortened voltage range over which emission zone movement is seen in these devices can be attributed to the high threshold voltages for electron and hole channel formation as derived using Equation 1. As can be seen in Equation 1, these threshold voltages

screen the gate voltage so that smaller gate voltages than those applied are induced in the channel region. The net result is that the gate voltage window over which the emission zone propogates is significantly reduced.

4. CONCLUSION

The capacitance of the gate dielectric, 9 nF/cm^2, is relatively small. In order to increase the brightness of the emission from an LEFET, a higher gate dielectric capacitance is needed. This can be achieved by using a thinner dielectric film and/or increasing the dielectric constant of the gate dielectric.

In conclusion, an ambipolar polymer light-emitting field-effect transistor using the top-contact, two-color electrode geometry (Ca as source and Ag as drain) has been demonstrated. Direct imaging of the emission zone within the channel region showed emission in a narrow region within the channel. The location of the emission zone is controlled by the gate bias. The emission zone is near the center of the channel at the crossover point where the electron and hole currents are equal. The gate bias induced shift in the emission zone, coupled with the ambipolar charge transport, indicates that the device is truly a light-emitting transistor.

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